A Compact and Low-Phase-Noise Ka-Band pHEMT-Based VCO

Belinda Piernas, Kenjiro Nishikawa, *Member, IEEE*, Tadao Nakagawa, *Member, IEEE*, and Katsuhiko Araki

***Abstract*—A low phase-noise Ka-band monolithic voltage-controlled oscillator (VCO) designed using the negative resistance concept is reported. A circuit fabricated using the three-dimensional monolithic microwave integrated circuit technology exhibits a high integration level; its size is a record at just 0.5 mm^2. On-wafer measurements demonstrate a low phase noise of −102 dBc/Hz at a 1-MHz offset. The VCO delivers an output power of 11.8 dBm at the center frequency of 28.3 GHz. The frequency tuning range is more than 3.8 GHz. Dependence of the circuit performance on the bias conditions is also reported and suggests that optimum phase-noise characteristic can be achieved when biasing the transistor to optimize its transconductance and noise figure.**

***Index Terms*—Three-dimensional (3-D) monolithic microwave integrated circuit (MMIC) technology, broad-band operation, phase noise, voltage-controlled oscillator (VCO).**

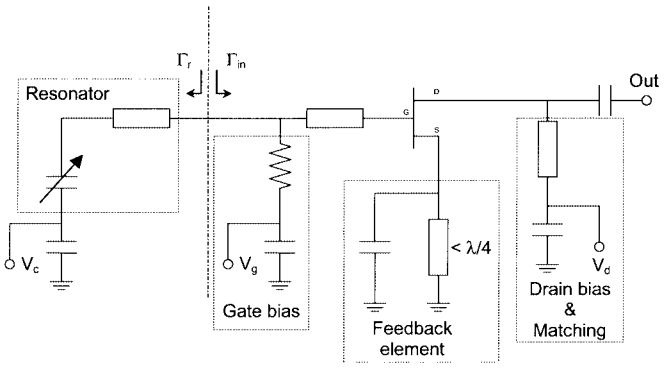

Fig. 1. Circuit schematic of a Ka-band VCO.

I. Introduction

THE strong continuous development of wireless communication systems has increased demand for compact, low-cost, widely tunable, and low-phase-noise oscillators with sufficient output power; it should be possible to directly use them in single-chip transceivers. Among all these requirements, the most critical one is the phase-noise performance. Stabilization of the oscillation frequency with a dielectric resonator (DR) has already been demonstrated, even at millimeter-wave frequencies, to be very effective in achieving a low-phase-noise characteristic [1]–[3]. This approach, however, does not permit full monolithic integration and requires extreme care in placing the resonator. Therefore, in terms of cost, reliability, and integration level, fully monolithic self-oscillating voltage-controlled oscillators (VCOs) are preferred.

In this paper, we report on the design, fabrication and performance of a monolithic low-phase-noise Ka-band VCO using an ultralow-noise pseudomorphic high electron-mobility transistor (pHEMT) technology and the three-dimensional (3-D) monolithic microwave integrated circuit (MMIC) technology. Though HBT technology, and more specifically InP-based HBT technology, is preferable from the viewpoint of low-frequency noise [4], high electron-mobility transistor (HEMT) technology is selected here because of its suitability for multifunctional applications when integrated into single-chip. A commercially available 0.15-μm ultralow-noise pHEMT technology developed by United Monolithic Semiconductor S.A.S. (UMS) was used to achieve the best phase-noise performance yet reported.

The monolithic pHEMT VCO delivers a typical output power of 11.8 dBm at the center frequency of 28.3 GHz with a tuning range of more than 3.8 GHz. On-wafer phase-noise measurement recorded −102 dBc/Hz at a 1-MHz offset. This Ka-band VCO's signal can be easily doubled for use in future V-band single-chip transceivers dedicated to high-speed wireless local area networks (LANs), image data transmission, contactless ID cards, and wireless vehicle and traffic information systems [5], [6].

The dependence of performance on bias conditions is also examined and confirms our initial predictions on optimum phase-noise performance.

II. Oscillator Configuration and Design

Fig. 1 shows the circuit schematic of the Ka-band VCO. The design is based on the negative resistance concept using a common-source series feedback element to generate the negative resistance. The active device is a 4 × 30 μm pseudomorphic HEMT based on 0.15-μm UMS PH15 ultralow-noise technology. The transition frequency f_T and the maximum oscillation frequency $f_{\max}$ of this transistor are 110 and 180 GHz, respectively. pHEMT size was optimized in order to achieve low-phase-noise performance. The transistor used here realizes a noise figure of 0.9 dB at 60% of Idss and 30 GHz. Gate and drain biases of the transistor were chosen to achieve a good compromise between noise figure performance and optimum g_m of the transistor. Biasing of the transistor near its maximum g_m enables the device to maintain relatively constant output power when the oscillation frequency is tuned. Moreover, as suggested

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B. Piernas was with the NTT Network Innovation Laboratories, NTT Corporation, Kanagawa 239-0847, Japan. She is now with Fujitsu Compound Semiconductor Inc., San Jose, CA 95131-1138 USA (e-mail: bpiernas@fcsi.fujitsu.com).

K. Nishikawa, T. Nakagawa, and K. Araki are with the NTT Network Innovation Laboratories, NTT Corporation, Kanagawa 239-0847, Japan (e-mail: nisikawa@wslab.ntt.co.jp).

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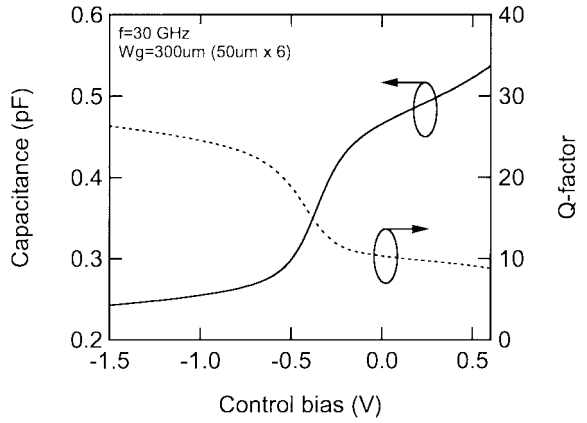

Fig. 2. Capacitance and Q-factor of a pHEMT transistor as a varactor.

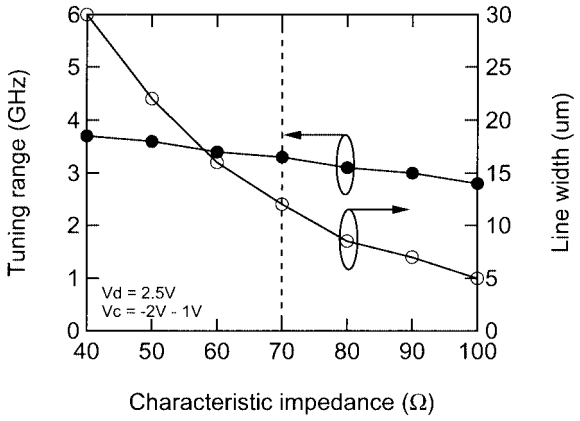

Fig. 3. Tuning range of the VCO versus characteristic impedance of a resonator.

by the results of Section V, this bias configuration corresponds to optimization of the phase-noise characteristic.

The feedback element that generates instability in the VCO consists of a short stub in parallel with a small capacitance. The short stub employs a 70-Ω transmission line to obtain both compactness and high inductance. A 60-Ω transmission line is used at the gate side to establish the required negative conductance and meet the oscillation condition [7]

$$|\Gamma_r| > \frac{1}{|\Gamma_{in}|} \tag{1}$$

$$\mathrm{Arg}\,(\Gamma_r) = \mathrm{Arg}\left(\frac{1}{\Gamma_{in}}\right). \tag{2}$$

The resonance circuit on the gate side consists of a transmission line in series with a variable capacitance to provide frequency tuning. The variable capacitance is implemented by a common drain–source transistor whose capacitance is controlled by the gate voltage. The gate width of this pseudomorphic HEMT is 300 μm. Fig. 2 shows the simulated capacitance and the corresponding Q-factor for the pseudomorphic HEMT varactor. The capacitive tuning range with a control voltage range of -1.5–0.6 V is roughly 2.3 : 1. In addition, the Q-factor at the control voltage of -1.5 V is 27 at 30 GHz. The conventional approach to implementing the variable capacitance is to use a varactor diode such as a Schottky varactor diode. However, varactor-tuned oscillators suffer from a relatively higher phase noise than fixed frequency oscillators due to the series resistance of the former. Moreover, the required varactor control voltage range to cover the entire frequency tuning bandwidth of the VCO is quite large. Fig. 3 shows the dependence of the simulated frequency tuning range on the characteristic impedance of the resonance transmission line. The corresponding line width of the resonator is also plotted in this graph. The control bias range of the varactor is -2–1 V. The tuning range of the VCO linearly increases with the decrease in the characteristic impedance of the resonator. A 70-Ω transmission line with a line width of 12 μm was chosen to realize both wider frequency tuning range and compactness. The loss and effective dielectric constant of the 70-Ω line are 0.19 dB/mm and 2.74, respectively.

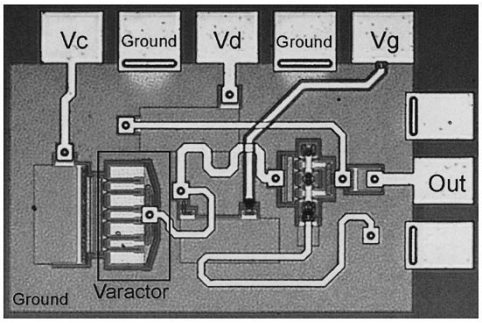

Fig. 4. Microphotograph of the Ka-band VCO.

In order to reduce the chip size, the output matching circuit also employs a 70-Ω transmission line in parallel. All transmission lines have a meander shape (see Fig. 4). The drain biasing circuit of the oscillating transistor is designed as an integral part of the output matching network. Gate bias of the transistor is provided through a small-size, high-impedance resistor.

III. VCO Fabrication

Fig. 4 shows a microphotograph of the fabricated Ka-band VCO. In order to realize a high-performance active device that also offers a high integration level, the proposed VCO was fabricated by combining the UMS PH15 process and the NEL 3-D interconnection process [8] that was developed by NTT Laboratories. This approach, first proposed in [9], offers a high integration level and high design flexibility; it provides the designer with the freedom to choose the active device process according to the performance and cost requirements.

The 3-D interconnection process is used to overlay UMS PH15 devices (transistor, resistor, and MIM capacitor) on a GaAs substrate. The 3-D interconnection process consists of four 2.5-μm-thick polyimide layers and four gold metal layers interfaced with the polyimide layers. The gold metal layers are 1 μm thick except for the top-level gold metal layer, which is 2 μm thick to benefit from lower loss. These gold metal layers implement the thin-film micro-strip (TFMS) transmission lines used to interconnect the devices of the UMS PH15 process and the passive structures and provide easy access lines for bias circuits.

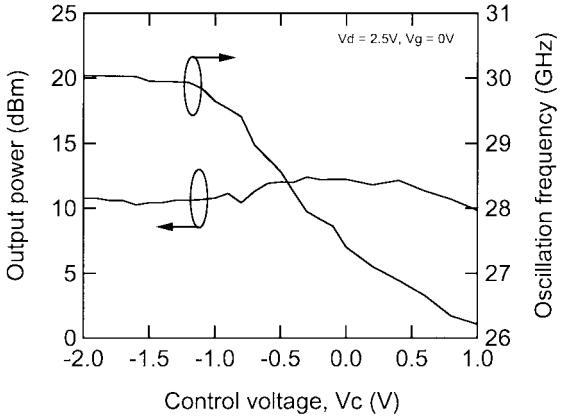

Fig. 5. Measured output power and oscillation frequency of the VCO versus the control voltage Vc applied to the varactor.

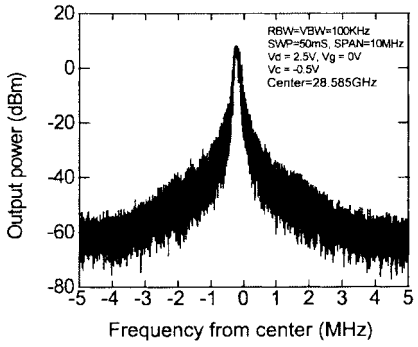

Fig. 6. Close-in spectral measurement of the VCO: $Vc = -0.5$ V.

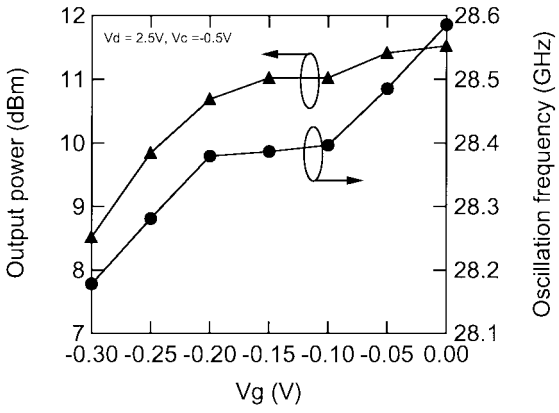

Fig. 7. Measured output power and oscillation frequency of the versus the gate voltage Vg.

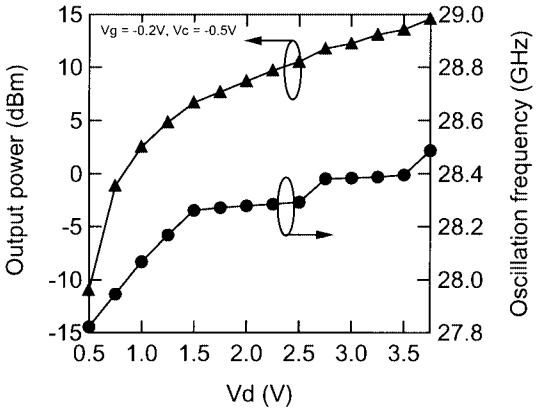

Fig. 8. Measured output power and oscillation frequency of the versus the drain voltage Vd.

The conductor layer of the UMS PH15 process, generally used for device interconnection, serves here as a ground plane for the 3-D interconnection process.

Narrow line width, tight spacing, and stacked structure are the key points of the 3-D MMIC technology. The realization of these features means that the proposed VCO achieves the very small chip size of 0.5 mm^2.

IV. Experimental Results

The VCO has been characterized on wafer, using an Agilent 8565E spectrum analyzer, in terms of oscillation frequency, output power, and phase noise.

Fig. 5 shows the measured oscillation frequency and output power of the VCO versus the controlled voltage Vc applied on the variable capacitor; the applied bias voltages were $Vd = 2.5$ V and $Vg = 0$ V. The power consumption is 80 mW. As already mentioned in Section II, these biases were chosen to reach the optimum g_m of the transistor, thus leading to the relatively constant output power of the VCO. Measured output power is 11.3 ± 1.2 dBm on a large frequency tuning range of 3.8 GHz. Center oscillation frequency is 28.3 GHz with a corresponding output power of 11.8 dBm. Fig. 6 shows the close-in spectral measurement of the VCO at the varactor's control voltage Vc of -0.5 V. The connection cable losses were not calibrated for these measurements. The self-oscillating oscillator exhibited remarkable stability and low phase noise were observed, even at $Vc = -0.5$ V where the frequency quickly grows with the controlled voltage of the varactor. Second-harmonic suppression of more than 15 dB was observed over the measured frequency range and there were no parasitic oscillations. In this bias condition, low phase-noise performance, -102 dBc/Hz and -68 dBc/Hz, were measured at 1-MHz and 100-kHz offsets (cf. Fig. 12).

Fig. 7 shows the dependence of the output power and oscillation frequency of the VCO on the gate bias Vg measured with $Vd = 2.5$ V and $Vc = -0.5$ V. The measured voltage range of the gate bias is -0.3–0 V. The output power quickly increases when the gate bias varies from -0.3 to -0.15 V. The output power slightly changed above the value of $Vg = -0.15$ V. The oscillation frequency deviation is about 400 MHz for the measured gate voltage range. Fig. 8 shows the dependence of the output power and oscillation frequency of the VCO on the transistor drain bias Vd measured with $Vg = -0.2$ V and $Vc = -0.5$ V. The range of the drain voltage is 0.5–3.75 V. The maximum measured output power was 14.6 dBm and the power control level of 7.9 dBm was obtained when varying the drain bias Vd from 1.5 to 3.75 V. Frequency pulling occurs at drain voltages under 0.5 V. For drain voltages Vd between 1.5 and 3.75 V, the oscillation frequency deviation is less than 230 MHz.

A comparison against state-of-the-art Ka-band VCOs (see Table I) shows that the proposed VCO exhibits competitive performance in terms of phase oise compared to HBT-based VCOs;

TABLE I
STATE-OF-THE-ART Ka-BAND VCOS

Technology	Chip size (mm^2)	Center Osc. Freq. Fc (GHz)	Tuning range (GHz)	Output power @ Fc (dBm)	Phase noise @ 100 kHz offset (dBc/Hz)	Phase noise @ 1 MHz offset (dBc/Hz)	Ref.
0.25 μm MESFET	3	38.25	0.5	12	-75	-95	[10]
0.25 μm HEMT	3.5	29.85	2.3	11	-70	—	[11]
0.2 μm Depletion HEMT	4	29.6	1.2	12	—	—	[12]
0.2 μm PHEMT	3.2	38.45	2.4	< 0	-63	—	[13]
0.2 μm PHEMT	2.25	33.75	0.35	9.4	—	—	[14]
0.18 μm PHEMT	—	29.3	0.55	0	-62	—	[15]
0.15 μm PHEMT	**0.5**	**28.3**	**3.8**	**11.8**	**-68**	**-102**	**This work**
GaInP/GaAs HBT	—	36.75	1.1	2.3	-80	-107	[16]
AlInAs/InGaAs HBT	3.2	38.4	0.85	10 (with Buffer)	-82	-107	[4]

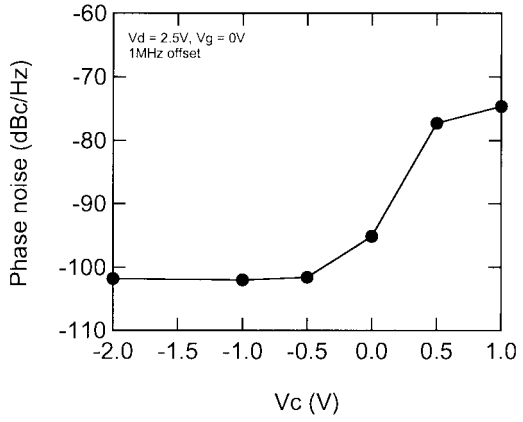

Fig. 9. Measured dependence of the phase noise on the control voltage Vc.

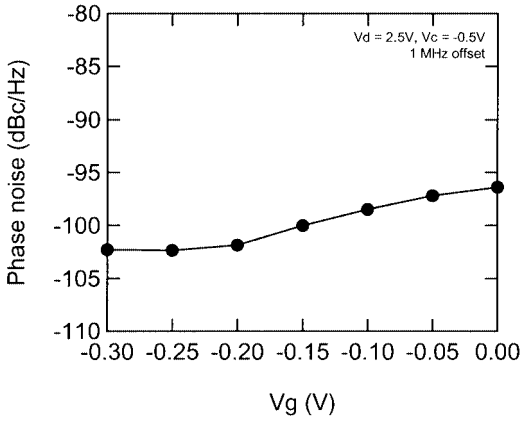

Fig. 10. Measured dependence of the phase noise on the gate voltage Vg.

its output power is among the highest values published. Moreover, it also offers significantly better frequency tuning range and chip size.

V. DEPENDENCE OF PHASE NOISE ON BIAS CONDITIONS AND DISCUSSION

In this section, we describe the measured phase-noise performance and its dependence on bias conditions. The measured bias conditions are those shown in Section IV.

Figs. 9–11 show the measured dependencies of the phase noise on the bias voltages at a 1-MHz offset. Fig. 9 shows the dependence of the phase noise on the control voltage Vc. Vd and Vg are 2.5 and 0 V, respectively. The measured phase noises are minimized to around −102 dBc/Hz over the voltage range of −2 to −0.5 V. At control voltages over −0.5 V, the phase noise increases with degradation of the varactor's Q factor. Fig. 10 shows the dependence of the phase noise on the gate voltage Vg with $Vc = -0.5$ and $Vd = 2.5$ V. The results show that the minimum phase-noise performance, around −102 dBc/Hz, is realized at the gate voltage range of −0.3 to −0.2 V. That region also realizes the minimum noise figure performance. Fig. 11 shows the measured dependence of the phase noise on the drain voltage Vd with $Vg = -0.2$ and $Vc = -0.5$ V. The minimum phase-noise value, −102 dBc/Hz,

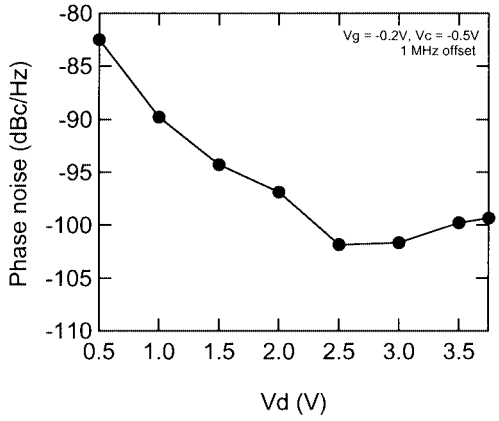

Fig. 11. Measured dependence of the phase noise on the drain voltage Vd.

was achieved at a drain bias Vd of 2.5–3.0 V, which corresponds to the maximum transistor transconductance g_m. Fig. 12 shows the phase-noise performance as a function of the offset frequencies away from the center frequency. The fabricated VCO MMIC achieves −68 dBc/Hz at a 100-kHz offset and −102 dBc/Hz at a 1-MHz offset. These phase-noise performances are excellent for full monolithic Ka-band VCO MMICs that offer a wide tuning range and high output power levels.

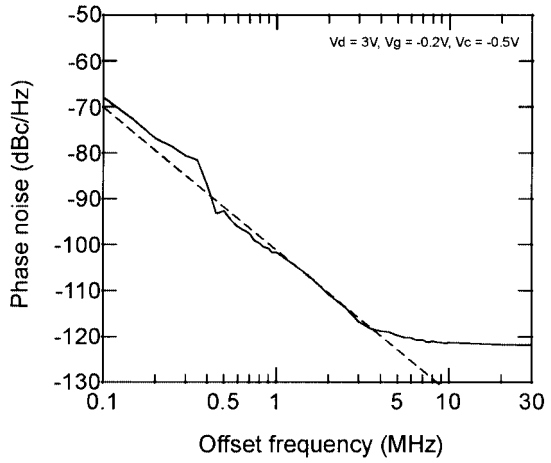

Fig. 12. Phase-noise measurement versus the offset frequency.

These results suggest that the phase-noise characteristic is minimized if the oscillating transistor is biased so as to yield the optimum transconductance characteristic (via the drain voltage) and optimum noise figure (via the gate voltage). The fabricated VCO also minimizes the phase-noise characteristic over one half of the available frequency tuning range.

Zhang [18] reported that the minimized up-conversion factor and phase-noise characteristic of HEMT devices were obtained at $Id/I\mathrm{dss}$ values from 0.8 to 1 when its gate condition was varied. However, our results on the gate voltage variation indicate that the minimum phase noise is realized at $Id/I\mathrm{dss}$ values from 0.6 to 0.8 ($Vg = -0.3$ to -0.2 V); that bias condition is the same as that yielding the optimum noise figure performance. We can guess that this is due to the ultralow-noise performance of the HEMT used. The minimum phase noise characteristic at high drain voltages may strongly depend on the nonlinearity of the transconductance (up-conversion of $1/f$ noise), resulting in the same behavior as the transconductance characteristic, which depends on the drain bias conditions. We confirmed that the nonlinear response of the phase noise to changes in the control voltage is due to the nonlinearity of the varactor's capacitance. The phase-noise characteristic was also improved with the Q-factor of the varactors.

VI. Conclusion

This paper demonstrated an ultracompact and low-phase-noise Ka-band monolithic VCO fabricated using the 3-D MMIC technology and a 0.15-μm ultralow-noise pHEMT technology. The VCO delivers an output power of 11.8 dBm at the center frequency of 28.3 GHz with a frequency tuning range of more than 3.8 GHz. A very small chip size (0.5 mm^2) is demonstrated thanks to the significant advantages of the 3-D MMIC technology.

The dependence of phase-noise characteristic on the pHEMT bias conditions was examined and the results suggest that optimum phase-noise performance can be achieved by biasing the transistor so as to achieve the optimum transconductance characteristic (via the drain voltage) and the optimum noise figure characteristic (via the gate voltage). The low phase noise of -102 dBc/Hz demonstrated at a 1-MHz offset makes this device competitive with HBT-based VCOs.

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Belinda Piernas was born in Sete, France, in 1972. She graduated from the Institut Supérieur d'Electronique du Nord, Lille, France, in 1995, and received the Ph.D. degree from the Institut National des Sciences Appliquées de Remes, Remes, France, in 1999.

In 1995, she joined the Optoelectronic Laboratory, Institut Supérieur d'Electronique de Bretague, Brest, France, where she was engaged in the design and fabrication of an optoelectronic self-routing cell switch. Her activity also included the design and fabrication of high-speed optoelectronic integrated circuits based on vertical-cavity surface-emitting lasers, MMICs, and optical interconnections. In 1999, she joined the NTT Network Innovation Laboratories, Yokosuka, Japan, where she was engaged in the design, using 3-D MMIC technology, of wireless communication integrated circuits for the future high-speed communication systems. She designed and developed millimeter-wave single-chip transceivers, including all functionally of the receiver and the transceiver block up to the antennas. In 2001, she joined Fujitsu Compound Semiconductor Inc., San Jose, CA. She is currently involved in the design of high-linearity and low-noise monolithic millimeter-wave integrated circuits for wireless communication systems.

Dr. Piernas was the recipient of the 2001 Young Engineer Award presented by the Institution of Electrical Engineers of Japan.

Kenjiro Nishikawa (A'93–M'00) was born in Nara, Japan, in 1965. He received the B.E. and M.E. degrees in welding engineering from Osaka University, Suita, Japan, in 1989 and 1991, respectively.

In 1991, he joined the NTT Radio Communication Systems Laboratories (now NTT Network Innovation Laboratories), Yokosuka, Japan. He has been engaged in research and development on 3-D and uniplanar MMICs on Si and GaAs, and their applications. His current interests are millimeter-wave MMIC design/packaging techniques and microwave/millimeter-wave communication systems.

Mr. Nishikawa is a member of the Institute of Electrical, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1996 Young Engineer Award presented by the IEICE.

Tadao Nakagawa (M'92) received the B.E. and M.E. degrees in material physics and the Dr.Eng. degree in communication engineering from Osaka University, Osaka, Japan, in 1986, 1988, and 1997, respectively.

In 1988, he joined NTT Radio Communication Systems Laboratories, Yokosuka, Japan, where he was engaged in research and development on MMICs and microwave synthesizers. From 1997 to 1999, he was an Associate Manager with the STE Telecommunication Engineering Company Ltd., where he was a Technical Consultant on wireless communications to the Seiko Epson Corporation, Nagano, Japan. Since 1999, he has been a Senior Research Engineer with NTT Network Innovation Laboratories, Yokosuka, Japan. He is currently involved in the design of multiband transceivers and millimeter-wave transceivers. Since 2001, he has also been a Part-Time Instructor with the Kanto Gakuin University, Yokohama, Japan. Since May 2002, he has been an Associate Editor for the *IEICE Transactions on Electronics.*

Dr. Nakagawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1995 Young Engineer Award presented by the IEICE.

Katsuhiko Araki received the B.E. and M.E. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1979 and 1981, respectively.

In 1981, he joined NTT Electrical Communications Laboratories, Yokosuka, Japan, where he has been engaged in research on GaAs monolithic microwave circuits and in the development of communication satellite onboard transponders. He is currently a Senior Research Engineer, Supervisor with NTT Network Innovation Laboratories, Yokosuka, Japan.

Mr. Araki is a member of the American Institute of Aeronautics and Astronautics (AIAA) and the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 1988 Sinohara Prize presented by the IEICE.